**IN THE CLAIMS:**

Please amend claims 1, 9 through 25 and 30 as follows:

1. (Currently Amended) A method comprising:

providing an instruction to access valid data in a cache and to indicate that a line storing the valid data in the cache is a candidate for replacement by reducing an importance level of the line after the valid data is accessed while maintaining the line as a valid line.

2. (Previously Presented) The method as recited in claim 1 further comprising:

reducing an importance level of the line based on the instruction.

3. (Previously Presented) The method as recited in claim 2 wherein the reducing of the importance level of the line results in the line being replaced prior to an other line scheduled for replacement by a replacement policy of the cache.

4. (Previously Presented) The method as recited in claim 3 wherein the replacement policy is a least recently used policy and wherein said other line is less recently used than the line.

5. (Previously Presented) The method as recited in claim 1 further comprising:

altering an allocation methodology of the cache based on the instruction.

6. (Previously Presented) The method as recited in claim 1 wherein the instruction is part of an application kernel.

7. (Original) The method as recited in claim 1 wherein the instruction is generated by a compiler.

8. (Original) The method as recited in claim 1 wherein the instruction is an extension of a memory access instruction.

9. (Currently Amended) ~~An~~ A machine-readable medium having stored thereon an instruction to perform a method comprising:

accessing ~~instruction comprising~~ a valid data memory ~~access~~ component and ~~an indication~~indicating that a line storing valid data in a memory of a cache is a candidate for replacement by reducing an importance level of the line while maintaining the line as a valid line.

10. (Canceled) ~~The instruction as recited in claim 9 wherein the indication causes a reduction of the importance level of the line.~~

11. (Currently Amended) The ~~instruction~~ machine-readable medium as recited in claim [[10]]9 wherein the reducing of the importance level of the line results in the line being replaced prior to an other line scheduled for replacement by a replacement policy of the cache.

12. (Currently Amended) The ~~instruction~~ machine-readable medium as recited in claim 11 wherein the replacement policy is a least recently used policy and wherein said other line is less recently used than the line.

13. (Currently Amended) The ~~instruction~~ machine-readable medium as recited in claim 9 further comprising:

altering an allocation methodology of the cache based on the instruction.

14. (Currently Amended) The ~~instruction~~ machine-readable medium as recited in claim 9 wherein the instruction in part of an application kernel.

15. (Currently Amended) The ~~instruction~~ machine-readable medium as recited in claim 9 wherein the instruction is generated by a compiler.

16. (Currently Amended) The ~~instruction~~ machine-readable medium as recited in claim 9 wherein the instruction is an extension of a memory access instruction.

17. (Currently Amended) A machine-readable medium having stored thereon a plurality of executable instructions to perform a method comprising:

providing an instruction to access valid data in a cache and to indicate that a line storing the valid data in the cache is a candidate for replacement by reducing an importance level of the line after the valid data is accessed while maintaining the line as a valid line.

18. (Currently Amended) The ~~article~~ machine-readable medium as recited in claim 17 wherein the ~~set of instructions~~method further comprises:

reducing an importance level of the line based on the indication.

19. (Currently Amended) The ~~article~~ machine-readable medium as recited in claim 18 wherein the reducing of the importance level of the line results in the line being replaced prior to an other line scheduled for replacement by a replacement policy of the cache.

20. (Currently Amended) The ~~article~~ machine-readable medium as recited in claim 19 wherein the replacement policy is a least recently used policy and wherein said other line is less recently used than the line.

21. (Currently Amended) The ~~article~~ machine-readable medium as recited in claim 17 the method further ~~comprising~~comprises:

altering an allocation methodology of the cache based on the indication.

22. (Currently Amended) The ~~article~~ machine-readable medium as recited in claim 17 wherein the indication is part of an application kernel.

23. (Currently Amended) The ~~article~~ machine-readable as recited in claim 17 wherein the indication is generated by a compiler.

24. (Currently Amended) The ~~article~~ machine-readable medium as recited in claim 17 wherein the indication is an extension of a memory access instruction.

25. (Currently Amended) A cache comprising:

a cache memory including a cache line storing valid data; and

a cache control logic to receive an instruction to access the valid data and an indication to reduce an importance level of the cache line based on the instruction while maintaining the cache line as a valid cache line.

26. (Original) The cache as recited in claim 25 wherein the instruction provides an indication that the cache line is a candidate for replacement.

27. (Original) The cache as recited in claim 26 wherein the cache control logic reduces an importance level of the cache line based on the indication.

28. (Original) The cache as recited in claim 27 wherein the reducing of the importance level of the cache line results in the cache line being replaced prior to another cache line scheduled for replacement by a replacement policy of the cache.

29. (Original) The cache as recited in claim 25 further comprising altering an allocation methodology of the cache based on the instruction.

30. (Currently Amended) A method for controlling a cache[,] comprising:

providing an instruction to access valid data in the cache and to indicate that a line storing the valid data is a candidate for replacement by reducing an importance level of the line; and

reducing an importance level of the line based on the instruction after the valid data is accessed while maintaining the line as a valid line.

Please add the following new claims as follows:

31. (New) The method as recited in claim 30 wherein the reducing of the importance level of the line results in the line being replaced prior to an other line scheduled for replacement by a replacement policy of the cache.

32. (New) The method as recited in claim 31 wherein the replacement policy is a least recently used policy and wherein said other line is less recently used than the line.

33. (New) The method as recited in claim 30 further comprising:

altering an allocation methodology of the cache based on the instruction.

34. (New) The method as recited in claim 30 wherein the instruction is part of an application kernel.

35. (New) The method as recited in claim 30 wherein the instruction is generated by a compiler.

36. (New) A processor comprising:

a decoder to receive a reduced importance cache line instruction to cause said processor to

access a valid data memory component, and

indicate that a line storing valid data in a memory of a cache is a candidate for replacement by reducing an importance level of the line while maintaining the line as a valid line.

37. (New) The processor of claim 36 wherein the reducing of the importance level of the line results in the line being replaced prior to an other line scheduled for replacement by a replacement policy of the cache.

38. (New) The processor of claim 36 wherein the replacement policy is a least recently used policy and said other line is less recently used than the line.

39. (New) The processor of claim 36 wherein said reduced importance cache line instruction is further to cause said processor to:

alter an allocation methodology of the cache based on the instruction.